A Power-Scalable Concurrent Cascade 2-2-2 SC ΣΔ Modulator for Software Defined Radio

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***Abstract*—This paper presents a flexible 1.2-V 90-nm CMOS cascade three-stage SC ΣΔ modulator with local resonation in the last two stages, unity signal transfer function and programmable (either 3 or 5 level) quantization in all stages. The chip reconfigures its loop filter order (2nd, 4th, 6th order), the clock frequency (from 40 to 240MHz) and scales the power consumption according to required specifications. These reconfiguration strategies are combined with the capability of concurrency in order to digitize up to three different wireless standards simultaneously. Experimental results demonstrate the flexibility of the proposed modulator, featuring a programmable noise shaping within a 100kHz-to-10MHz signal band, with adaptive power dissipation[1].**

I. Introduction

Next generation of Software-Defined-Radio (SDR) handheld terminals will require flexible Analog-to-Digital Converters (ADCs) capable to operate with a variable and increasing range of signal bandwidths and effective resolutions. In addition to reconfigure their performance with adaptive power dissipation, these ADCs must be able to handle different standards and operation modes concurrently [1].

State-of-the-art reconfigurable, multi-mode ADCs have been mainly implemented using ΣΔ Modulators (ΣΔMs) [2]–[5]. The widest conversion region in the resolution-vs-bandwidth plane is covered by [3] and [5], digitizing signal BandWidths (BWs) ranging from hundreds of kHz to 20MHz. To the best of the authors' knowledge, none of reported multi-standard ΣΔMs can be reconfigured to process either a single input signal or multiple signals concurrently. However, this is a common situation in the majority of mobile phones today and it is expected that SDR transceivers will handle a larger number of operating modes simultaneously.

This paper presents the first integrated ΣΔM that features both reconfiguration and concurrency capabilities. The chip covers the requirements of six wireless standards (GSM, Bluetooth, GPS, UMTS, DVB-H and WiMAX) in a direct-conversion receiver, and it is able to handle up to three of them simultaneously. Experimental measurements demonstrate these features, showing a high flexibility of the circuit to accommodate its performance to different signal conditions, while covering one of the widest regions in the resolution-vs-bandwidth plane.

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II. Modulator Architecture

Fig. 1 shows the block diagram of the proposed modulator. It consists of a reconfigurable 6th-order cascade 3-stage (2-2-2) ΣΔM. Unity Signal Transfer Function (USTF) is obtained through the use of feed-forward paths in each single-loop stage and local resonation is implemented in the second and third modulator stages. Multi-bit quantization is included in all stages with a number of levels programmable to either 3 or 5. Every stage can work either separately or as part of the cascade in order to allow both reconfigurability and concurrency operation with three possible input signals, X_1, X_2 and X_3. The Digital Cancellation Logic (DCL) – postprocessed by software in this prototype – is adjusted to match the corresponding ΣΔM configurations, namely:

- All stages operating in a 2-2-2 cascade ΣΔM, where the input signal is X_1 and the output signal is $Y_{2\text{-}2\text{-}2}$. In this case, DCL2 configuration is used.
- The first two stages connected in a 2-2 cascade topology, considering X_1, $Y_{2\text{-}2}$ and the DCL1 configuration. In this configuration, the last stage can be either switched off to save power or it can work in a single-loop configuration to process X_3 concurrently.
- The first stage operating as a 2nd-order single-loop ΣΔM, where the input and output signals are X_1 and Y_{1SL}, respectively. In this configuration, the back-end stages are connected together with DCL3 to implement a

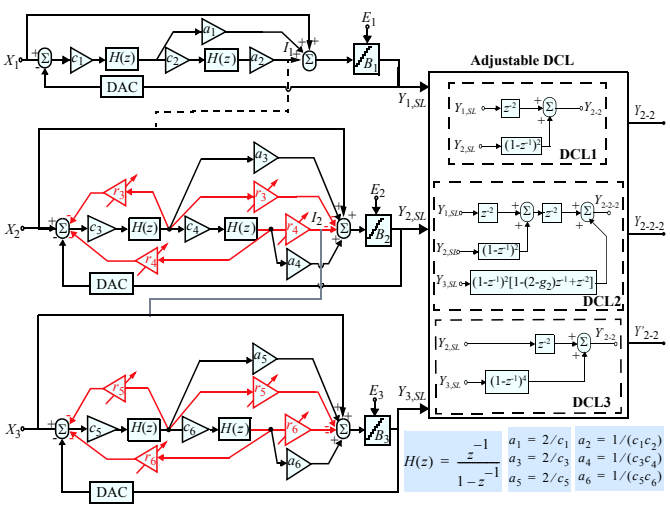


Fig. 1. Block diagram of the proposed ΣΔ modulator.

2-2 cascade ΣΔM, where the input and the output signals are respectively X_2 and $Y'_{2\text{-}2}$. This way, both X_1 and X_2 can be processed concurrently by a 2nd- and a 4th-order ΣΔM, respectively.

- All stages operating separately, so that the three inputs X_1, X_2, X_3 can be processed simultaneously and the modulator has three outputs: $Y_{1,SL}$, $Y_{2,SL}$ and $Y_{3,SL}$.

Assuming a linear model for the quantizers, it can be shown that the Noise Transfer Function (NTF) at the output of the i-th stage is given by:

$$\text{NTF}_{i,SL}(z) = 1 - (1 - g_i)z^{-1} + z^{-2} \tag{1}$$

where $g_1 = 0$, $g_2 = r_3/2$ and $g_3 = r_5/2$.

The NTF at the output of the different cascade configurations can be obtained by properly combining $\text{NTF}_{i,SL}(z)$ as:

$$\begin{aligned} \text{NTF}_{2\text{-}2} &= \text{NTF}_{1,SL}(z) \cdot \text{NTF}_{2,SL}(z) \\ \text{NTF}'_{2\text{-}2} &= \text{NTF}_{2,SL}(z) \cdot \text{NTF}_{3,SL}(z) \\ \text{NTF}_{2\text{-}2\text{-}2} &= \text{NTF}_{1,SL}(z) \cdot \text{NTF}_{2,SL}(z) \cdot \text{NTF}_{3,SL}(z) \end{aligned} \tag{2}$$

A. Modulator In-Loop Filter Coefficients

The modulator in-loop filter coefficients, $\{a_i, c_i\}$, were chosen to optimize the trade-off between the integrators Output Swing (OS) and the number of unit capacitors, considering a 1.2-V supply voltage. To this end, an exhaustive simulation-based exploration of the design space was carried out, taking into account only in-loop coefficient values that are power of 2 and that fulfill the relations given in Fig. 1. The result of this exploration gives a_i=4 and c_i=0.5, which – considering 5-level quantization – results in an OS$<$ 0.265V and OS$<$ 0.075V, respectively for the front-end and back-end integrators of each stage, i.e approximately 22% and 6% of the ΣΔM reference voltage, V_{ref} = 1.2V. The OS requirements are roughly doubled if a 3-level quantizer is used.

Local resonation is implemented in second- and third stages through $r_{3,4}$ and $r_{5,6}$ coefficients, respectively, where $r_4 = 2r_3$ and $r_6 = 2r_5$. In these stages, feed-forward coefficients are modified as $a'_i = a_i - r_i$, with $i \in [3, 6]$ and a_i denote the feed-forward coefficients when no resonation is operating, i.e $r_i = 0$. Coefficients $g_{2,3}$ in (1) are implemented through a switchable capacitor array so that their values can be independently programmed to four values each one, namely $g_2 = 0, 0.0625, 0.125, 0.250$ and $g_3 = 0, 0.1, 0.25, 0.35$, as well as all possible combinations among them.

B. SC Implementation

Fig. 2 shows the conceptual (single-ended) Switched-Capacitor (SC) schematic of the first and second stage of the modulator. The third stage – not shown in Fig. 2 for the sake of simplicity – is identical to the second stage. Different SC branches are connected at the input of the front-end integrators in both stages – depending on either a 3- or 5-level configuration is used for the quantizers. Thus, for instance, the SC branch corresponding to C_{s11} in the first stage is used for 3-level quantization, while C_{s21} and C_{s31} are also needed if 5-level quantization is used. Similarly, sampling

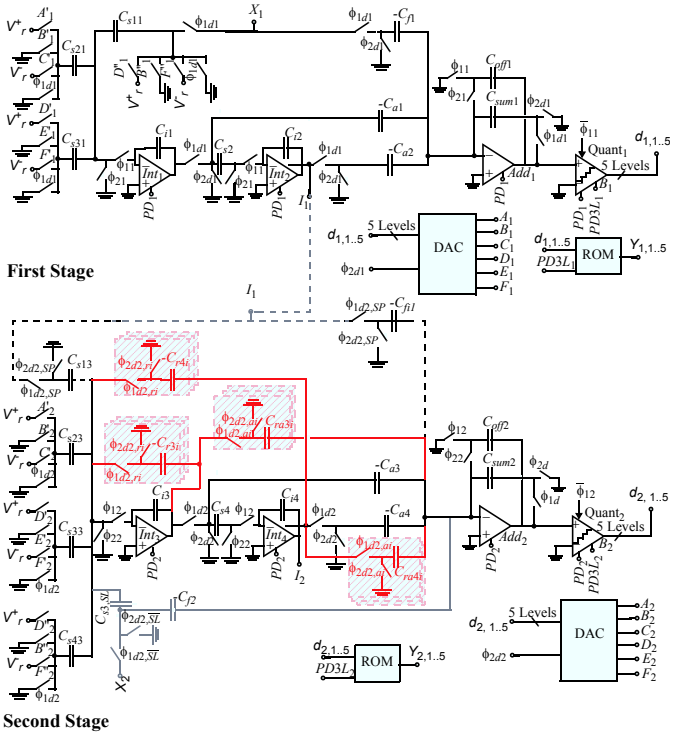


Fig. 2. Conceptual SC schematic of the modulator.

capacitors C_{si3} with $i = 1, 2, 3, 4$ are used in the second- and third- stages depending on the quantizer configuration.

Active analog adders have been used in the modulator. The signals to be added are sampled by the capacitors C_{fi}, C_{fij} and C_{ai}. Then, capacitor C_{sumi} performs the summation, while C_{offi} is employed to hold and subtract the opamp offset. A scaling factor of $\alpha = 1/4$ is implemented to reduce the output swing requirements of the active-adder opamp. This factor – which is later compensated by properly scaling the reference voltages of the quantizers – imposes a requirement on the offset of the comparators of 100 and 60 mV for $K = 3$ and $K = 5$, respectively, with K being the number of levels of the quantizers.

C. Control Logic for Reconfiguration and Concurrency

Fig. 3 depicts the digital logic blocks used to implement the main reconfiguration functionalities by means of a set of control signals. Thus, PD_i is used to power up/down the i-th stage and concurrent operation is governed by control signal SL_i. Control signals $PDRes_i < j >$ enable the resonation operation of the i-th stage and $PD3L_i$ sets the quantization resolution of the embedded ADC and the DAC. The activation of signal $PD3L_i$ sets $K = 5$ and otherwise $K = 3$.

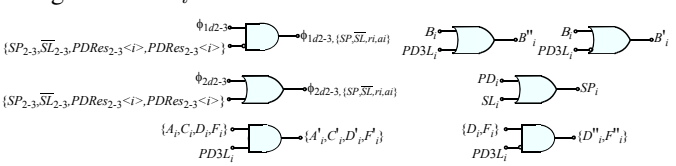


Fig. 3. Main parts of the reconfiguration digital control logic.

III. Circuit Design and Implementation

The ΣΔM has been designed to cope with the specifications of a direct-conversion receiver for GSM, Bluetooth, GPS, UMTS, DVB-H and WiMAX. This results in a requirement for the Signal-to-(Noise+Distortion) Ratio (SNDR) of 75-to-50 dB within a 0.2-to-10MHz BW, respectively [4].

A. Biasing Adaptability

In order to adapt the performance of the ΣΔM to the different specifications with optimized power consumption, the biasing of the main building blocks is adjusted by using the programmable master current generator shown in Fig. 4(a). The master current is generated through an external resistor, $R = 620\text{k}\Omega$, connected to a PMOS current mirror. A set of output currents are mirrored with unity factor and the effective transistor lengths in the NMOS mirrors are increased by placing transistors in series.

Reconfiguration is performed by using 5-bit binary-weighted PMOS current mirrors as shown in Fig. 4(b). All mirrored currents are selected by control signals, $Ctrl < i >$, applied to the gates of NMOS-based switches. These mirrored currents go directly to all analog blocks, so that they have a dedicated signal $Ctrl < i >$ to control their bias current independently.

B. Amplifiers Scalable Performance

Folded-cascode topologies were used for all the opamps in the modulator. Table I sums up the opamp worst-case simulated performance for different values of the bias current, I_B – obtained from a corner analysis that considers $\pm 5\%$ variation in the 1.2-V supply voltage, slow and fast device models and a temperature range of $[-40°\text{C}, +80°\text{C}]$. The adaptable dynamic behavior is shown based on the variation of the transconductance, g_m, the Gain-Bandwidth (GB) during

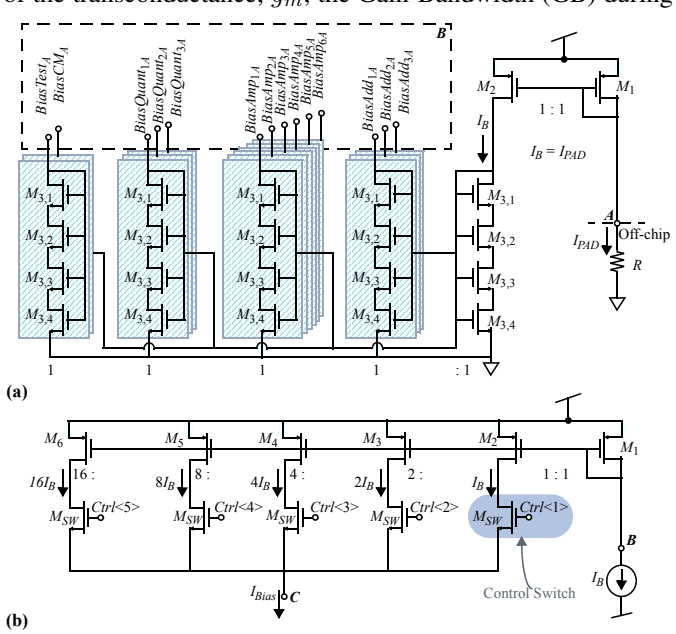
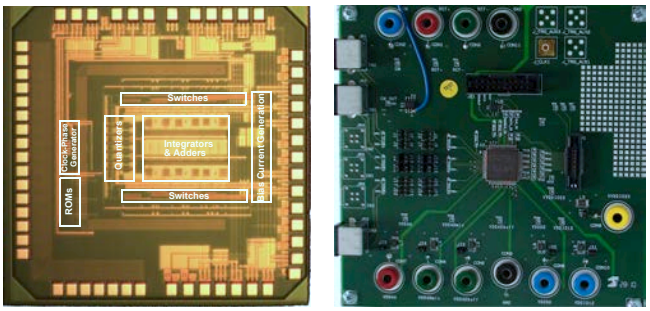


Fig. 4. Programmable biasing. (a) Master generator. (b) Reconfiguration.



(a) (b)

Fig. 5. Chip implementation. (a) Microphotograph. (b) Test PCB.

integration and sampling phases (GB_i and GB_s, respectively), the current at the opamp output branch, I_o, and the Slew-Rate (SR) in both clock phases.

IV. Experimental Results

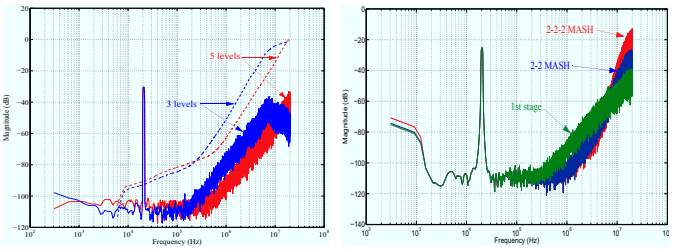
The modulator has been implemented and fabricated in a 90-nm 1-poly 9-metal digital CMOS technology. Fig. 5(a) shows the microphotograph, highlighting its main parts. The chip core occupies an active area of 2.3mm^2. The layout floorplan is based on extensive use of common-centroid techniques, capacitive decoupling, supplies and ground isolation of the different sections of the circuit. The digital part of the circuit includes the clock phase generator, the DACs, and the control signal generators. As a total of 90 control signals are required to implement the different reconfiguration techniques embedded in the chip, a serial-to-parallel register is used. To simplify the test, the output digital streams of each stage are stored in a ROM (see Fig. 2) and then captured off-chip.

The chip was mounted on a 64-pin ceramic QFP package and tested using the Printed Circuit Board (PCB) shown in Fig. 5(b), that includes the required antialiasing filtering for the input signals, as well as proper decoupling filtering for supplies and reference voltages. A logic analyzer was used to capture the output bit streams, which were transferred to a workstation and processed using MATLAB.

Fig. 6(a) shows the measured 256k-point Hanning-windowed FFTs of the modulator first-stage output, for 3- and 5-level quantization modes, considering a sampling frequency of $f_s = 40\text{MHz}$ and a 20-kHz input sinewave. The reconfiguration of the loop-filter order is illustrated in Fig. 6(b), where three different configurations are shown, namely:

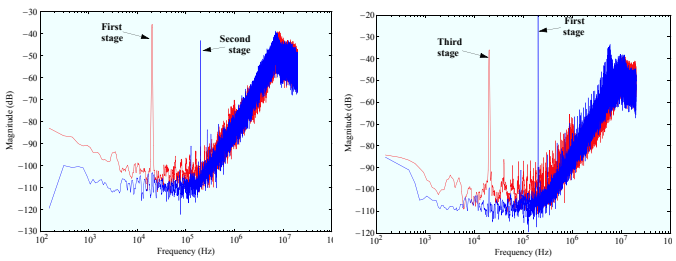
Table I: Worst-case Simulated Performance of the Opamps vs. Bias Current

I_B (μA)	5	10	20	30	40	50	60
DC gain (dB)	47.09	47.16	47.31	47.13	46.71	46.1	45.34
gm (mA/V)	1.02	1.71	2.77	3.66	4.35	4.87	5.46
GB_i (MHz)	524	878	1422	1879	2233	2500	2803
GB_s (MHz)	79	133	216	285	339	380	426
Phase margin (°)	68.54	70.19	71.91	73.02	73.65	74.09	74.61
Io (μA)	42.77	91.66	193.9	298.4	404.1	510.5	617.4
SR_i (V/μs)	57	125	269	417	571	726	884
SR_s (V/μs)	7	15	33	52	71	90	110
$C_{eq,i}$ (pF)	0.31						
$C_{eq,s}$ (pF)	2.04						
Input cap. (fF)	162.5	172.2	179.6	184.0	187.6	190.8	193.7
Output cap. (fF)	26.72	20.57	14.14	12.14	10.12	9.08	8.46
Output swing (V)	±0.96	±0.91	±0.83	±0.76	±0.7	±0.64	±0.59
Power (mW)	0.28	0.53	1.01	1.48	1.94	2.4	2.85



(a) (b)

Fig. 6. Reconfiguration of (a) Internal quantization. (b) Loop filter order.



(a) (b)

Fig. 7. Concurrent operation of (a) 1st and 2nd stages. (b) 1st and 3rd stages.

a 2nd-order single-loop, a 4th-order 2-2 cascade and a 6th-order 2-2-2 cascade.

One of the main characteristics of this chip is its capability to operate concurrently with different input signals. This is illustrated in Fig. 7(a) that shows the output spectra of the first and the second stages processing different input sinewaves at 20kHz and 200kHz, respectively. Similarly, Fig. 7(b) shows the simultaneous operation of the first and third stages.

The flexibility of the chip is based on the combination of reconfiguration, concurrency and power adaptation. The latter is illustrated in Fig. 8, where the power dissipation of the analog part (opamps and quantizers) is reconfigured by varying the control digital word of the on-chip binary-weighted current mirrors (see Fig. 4). The overall $\Sigma\Delta$ power consumption can be scaled down from 23.5mW to 7.6mW when the sampling frequency is varied from 240MHz to 40MHz, according to the different standard requirements.

Finally, Fig. 9 shows the measured output spectra corresponding to different operation modes, considering suitable configurations for each case. The effective resolution achieved

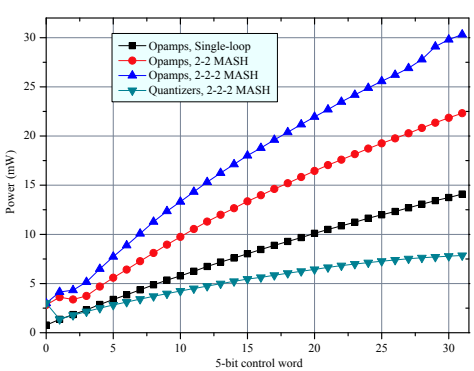


Fig. 8. Scaling power consumption of opamps and quantizers.

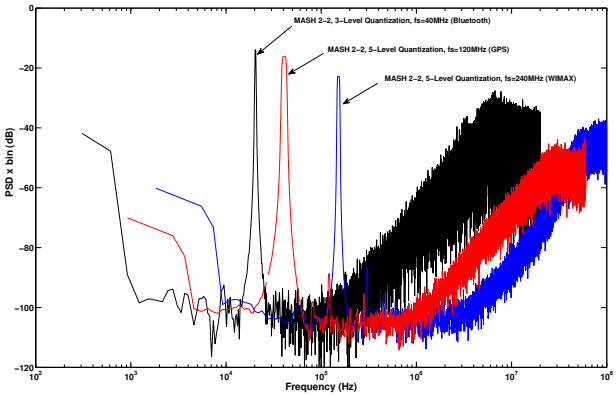


Fig. 9. Measured output spectra for different standards.

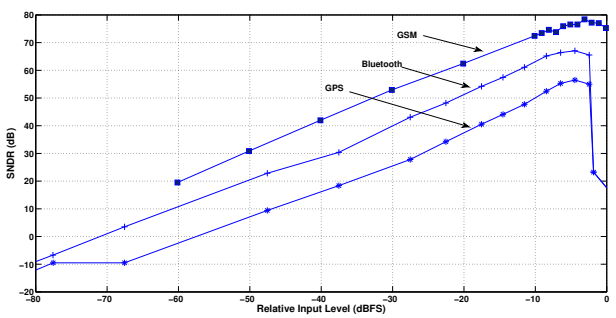


Fig. 10. SNDR vs. input amplitude for different operation modes.

by the chip is illustrated in Fig. 10, where SNDR is depicted versus the input signal amplitude for several standards.

V. Conclusion

A flexible 1.2-V 90-nm CMOS SC $\Sigma\Delta$M has been presented, which can be reconfigured to the requirements of different wireless standards with adaptive power dissipation. Compared to previously reported reconfigurable $\Sigma\Delta$Ms, this chip is the first one to incorporate the ability to operate concurrently with several signals. This novel characteristic makes the proposed $\Sigma\Delta$M a very suitable candidate for the implementation of ADCs in Software-Defined-Radio receivers.

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